In yet another embodiment, shown in FIG. 4, reading is done by reverse biasing of the NP junction between the doped region 12 and the well 11. The end A of the fuse is grounded, and the end B disconnected from the ground for purposes of reading the state of the fuse. To this end, it is necessary to provide, firstly, for an isolation transistor T1 between the terminal B and the ground and, secondly, a transistor T12 to connect the terminal A to the ground.

The transistor T1 is made conductive at the same time as T1 for the blowing of the fuse, both responsive to the blow-out signal CL. The transistor T1 is non-conductive for reading the state of the fuse. This transistor should be as big as the transistor T1 since it also carries the fuse blow-out current. If the transistor T1 is a P channel transistor and the transistor T1 is an N channel transistor, an inverter I1 receives the blow-out signal CL applied to T1 and reverses it to apply it to the control gate of T1.

The transistor T12 which is used to connect the terminal A to the ground may be a small N channel transistor. It carries only a small reading current. It is put into a state of conduction for the reading operation by a read signal LECT present outside periods reserved for the blowing out of the fuse.

The read circuit may be similar to that of FIG. 2, with a source SCL for the supply of current to the fuse through the terminal B and a simple threshold comparator CMPS connected to the terminal B to detect the logic level present at the terminal B. The threshold of the comparator is far less critically important than in the case of the reading when the junction is forward biased. It may be equal to about 2 volts for a 5-volt supply but the input is then the terminal B and not the terminal A of the fuse.

The read circuit could also be of the same type as that of FIG. 3 with, once again, a reversal of the terminals A and B and the addition of the transistors T1 and T12 to achieve this reversal of bias between reading and blowing.

Having thus described one particular embodiment of the invention, various alterations, modifications, and improvements will readily occur to those skilled in the art. Such alterations, modifications, and improvements are intended to be part of this disclosure, and are intended to be within the spirit and scope of the invention. Accordingly, the foregoing description is by way of example only and is not intended as limiting. The invention is limited only as defined in the following claims and the equivalents thereto.

What is claimed is:

1. A physical fuse circuit with a low blow-out voltage and a low blow-out current density for integrated circuits formed in a semiconductor substrate, including a circuit for blowing the fuse, comprising:

a shallow, doped first semiconductor region having a first conductivity type, diffused in a second semiconductor region having a second conductivity type that is opposite to the first conductivity type; and

a diffusion metal layer formed in direct contact with the doped first semiconductor region; wherein

the first semiconductor region has a depth of about 0.2 microns, and a voltage of about 3–5 Volts across the fuse produces a blow-out current with a current density substantially one milliampere per square micrometer at the diffusion metal layer.

2. The fuse according to claim 1, wherein the second semiconductor region is a well formed in the semiconductor substrate in which the integrated circuit is formed, the semiconductor substrate having a conductivity type opposite that of the second semiconductor region.

3. The fuse according to claim 1, wherein the diffusion metal layer is an aluminum layer.

4. The fuse circuit according to claim 1, wherein the doped region has a doping substantially in the range of 10^{18}–10^{20} atoms per cm^3.

5. The fuse according to claim 1, including a circuit for reading a fuse state, further comprising:

means for applying a low-value reading current to the fuse in a direction to forward bias a junction between the doped first semiconductor region and the second semiconductor region.

6. The fuse circuit according to claim 1, including a circuit for reading a fuse state, further comprising:

a threshold comparator having a threshold substantially equal to 0.3 volts, and producing an output signal indicative of whether a drop in voltage across the terminals of the fuse is greater than or less than the threshold.

7. The fuse according to claim 1, including a circuit for reading a fuse state, further comprising:

means for applying a low bias voltage to the fuse in a direction to forward bias a junction between the doped first semiconductor region and the second semiconductor region; and

means to convert a current through the fuse into a voltage.

8. The fuse circuit of claim 7, wherein the means to convert further comprises:

a current mirror connected to mirror into an output branch the current; and

a resistor in the output branch.

9. The fuse according to claim 1, including a circuit for blowing the fuse, further comprising:

means for applying a blow-out current to the fuse in a direction in which a junction between the doped first semiconductor region and the second semiconductor region is forward biased.

10. The fuse and circuit of claim 1, further comprising:

means for applying the blow-out current for several seconds.

11. The fuse of claim 1 including a circuit for blowing the fuse and further including a circuit for reading the fuse, further comprising:

means for applying a blow-out current to the fuse in a direction in which a junction between the doped first semiconductor region and the second semiconductor region is forward biased; and

means for applying a low-value reading current to the fuse in a direction in which the junction is reverse biased.

12. The fuse and circuits of claim 11, further comprising:

a threshold comparator whose input is connected to a first contact of the fuse, which further has a second contact connected to ground.

13. A physical fuse with a low blow-out voltage of about 3–5 Volts and a low blow-out current density of substantially one miliampere per square micrometer, formed in semiconductor substrate of an integrated circuit, comprising:

a junction formed of a shallow region of a depth of about 0.2 microns and of a first conductivity type in contact with a region of a second conductivity type; and

a diffusion metal layer disposed in direct contact with the shallow region, the metal selected to diffuse readily through the shallow region when a blow-out current passes through the metal.

14. The fuse of claim 13, wherein the semiconductor substrate is silicon.

15. The fuse of claim 13, in which the region of a second conductivity type is a well in which the shallow region is formed by diffusing a dopant therein.

16. The fuse according to claim 1, further comprising a circuit for blowing the fuse comprising means for applying across the fuse a low forward bias that is the voltage of about 3–5 Volts.

17. The fuse according to claim 1, wherein current through a fuse that is blown flows substantially through semiconductor regions of a single type.

18. The fuse according to claim 1, wherein the semiconductor substrate is silicon.

19. The fuse of claim 13, wherein the blow-out current has a blow-out current density of about 1 mA/μm^2.

20. The fuse of claim 13, further comprising a circuit for blowing the fuse by inducing a current density where the metal layer contacts the first region causing the metal to diffuse into the first region and thereby short-circuiting the junction.

21. The fuse of claim 20, wherein the metal is aluminum.

22. The fuse according to claim 13, further comprising a circuit for blowing the fuse comprising means for applying across the fuse a low forward bias that is substantially less than about 10 Volts.

23. The fuse of claim 19, wherein the shallow region has a depth of about 0.2 microns, and the fuse has a blow-out voltage of about 3–5 Volts.

24. The fuse of claim 13, wherein the shallow region has a doping substantially in a range of 10^{18}–10^{20} atoms per cm^3.

25. A physical fuse circuit with a low blow-out voltage and a low blow-out current density for integrated circuits formed in a semiconductor substrate, including a circuit for blowing the fuse, comprising:

a shallow, doped first semiconductor region diffused in a second semiconductor region; and

a diffusion metal layer formed in direct contact with the doped first semiconductor region; wherein

the first semiconductor region has a depth of about 0.2 microns, and a voltage of about 3-5 Volts across the fuse produces a blow-out current with a current density substantially one milliampere per square micrometer at the diffusion metal layer.